

BTeV Trigger (WBS 1.8)

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- Introduction and overview of the BTeV trigger
- **WBS 1.8**
 - Project description
 - Project organization
 - Technical details and progress since DOE CD-1 Review
 - Cost
 - Schedule
 - Milestones
 - Risk assessment
 - Response to DOE CD-1 recommendations
 - FY05 Project Plans and Status
- Presentations prepared for breakout sessions

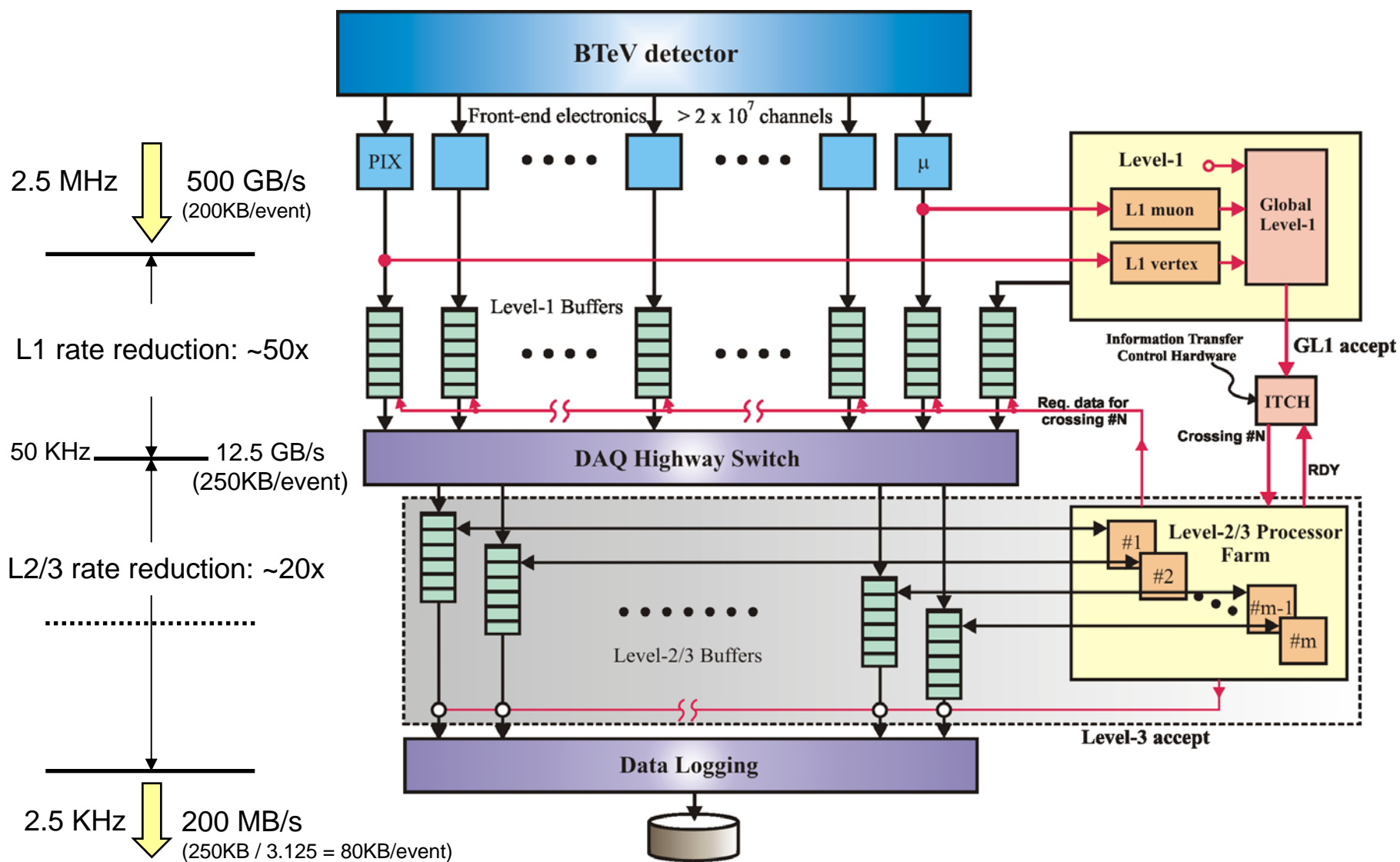
- The challenge for the BTeV trigger and data acquisition system is to reconstruct particle tracks and interaction vertices for **EVERY** interaction that occurs in the BTeV detector, and to select interactions with *B* decays.
- The trigger performs this task using 3 levels, referred to as Levels 1, 2, and 3:
 - “L1” – looks at every interaction and rejects at least 98% of min. bias background
 - “L2” – uses L1 computed results & performs more refined analyses for data selection
 - “L3” – rejects additional background and performs data-quality monitoring

Reject > 99.9% of background. Keep > 50% of *B* events.

- The data acquisition system saves all of the data in memory for as long as necessary to analyze each interaction, and moves data to L2/3 processing units and archival data storage for selected interactions.
- The key ingredients that make it possible to meet this challenge:
 - BTeV pixel detector with its exceptional pattern recognition capabilities
 - Rapid development in technology – FPGAs, processors, networking

Note: see glossary at the end of this talk

Block Diagram of Trigger & DAQ Data Flow



- L1 pixel trigger (FPGAs, L1 Switch, L1 Farm)
- L1 muon trigger (same hardware as L1 pixel trigger)
- Global Level 1 trigger (same processing hardware)
- L2/3 hardware (Linux PC farm)
- L2/3 software (track and vertex reconstruction for L2 & L3, and additional software for detector/data-quality monitoring)
- RTES software (fault detection and mitigation)

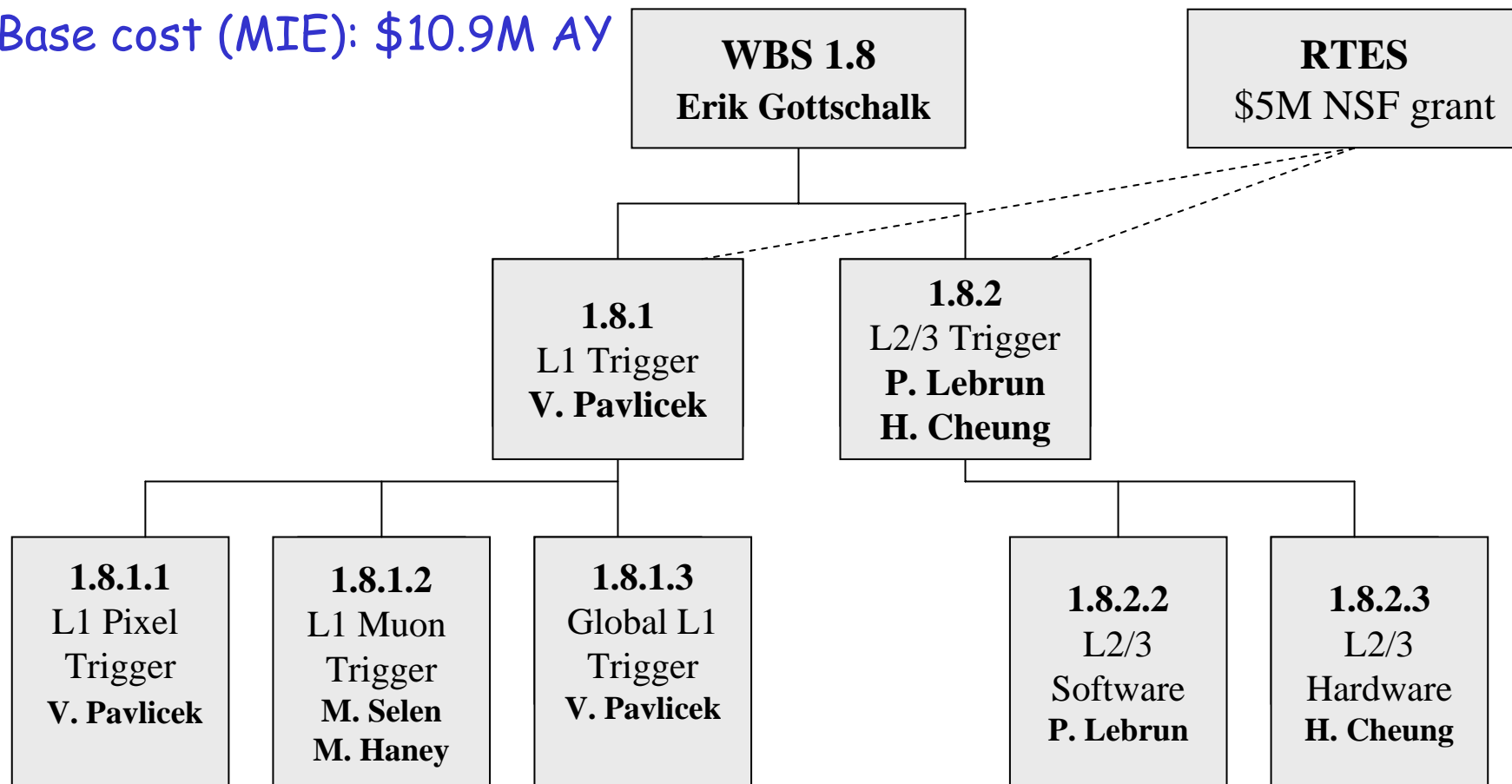
Base cost (FY05 dollars): \$11.4M (Material: \$7.8M, Labor: \$3.6M)

Base cost (MIE only): \$10.9M AY

+ \$5M grant for RTES (NSF ITR program)

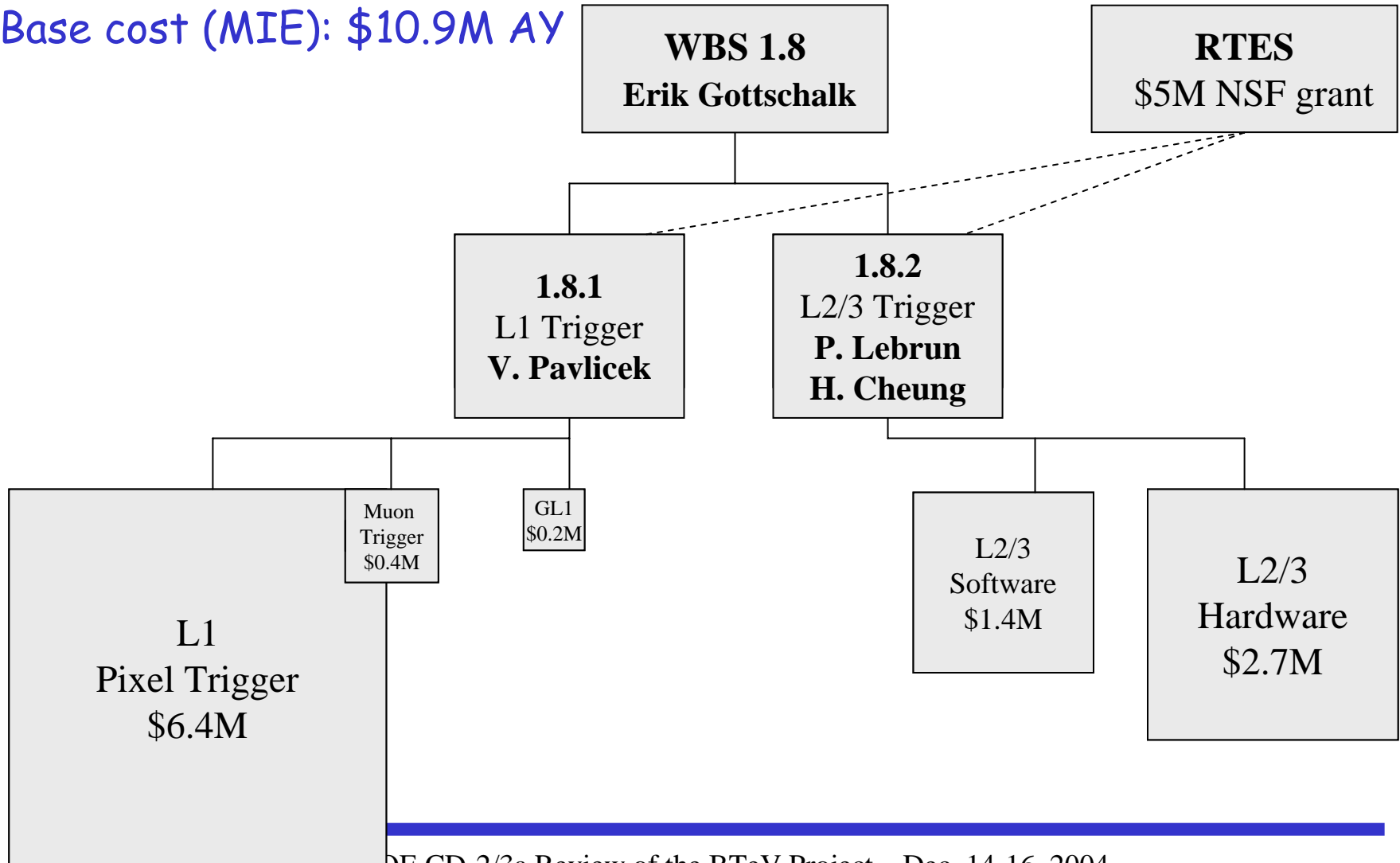
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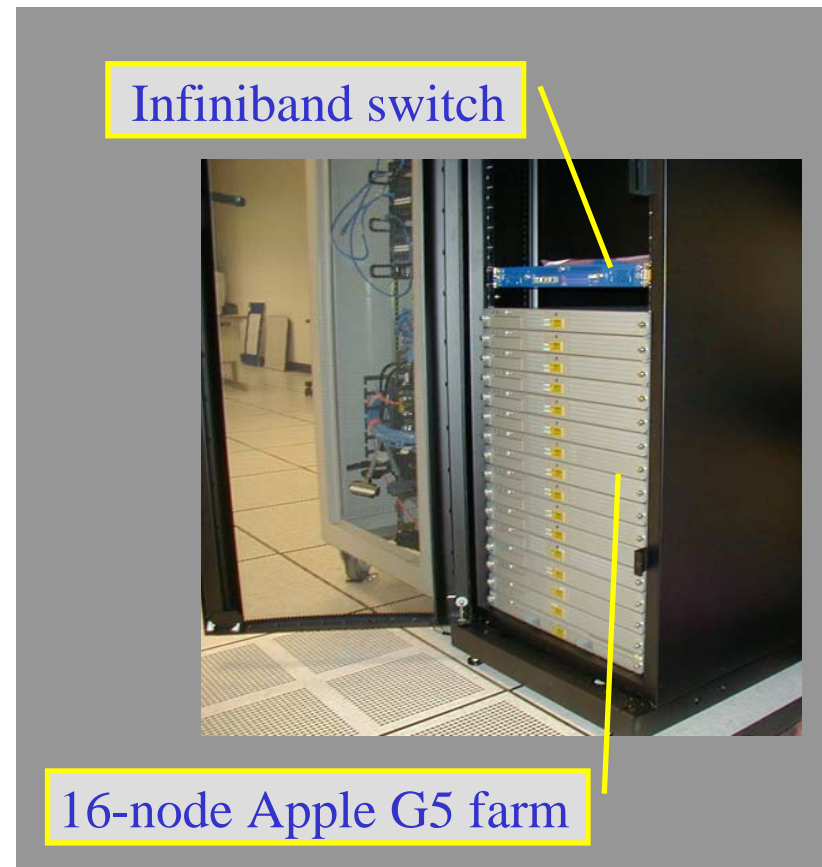
Base cost (MIE): \$10.9M AY



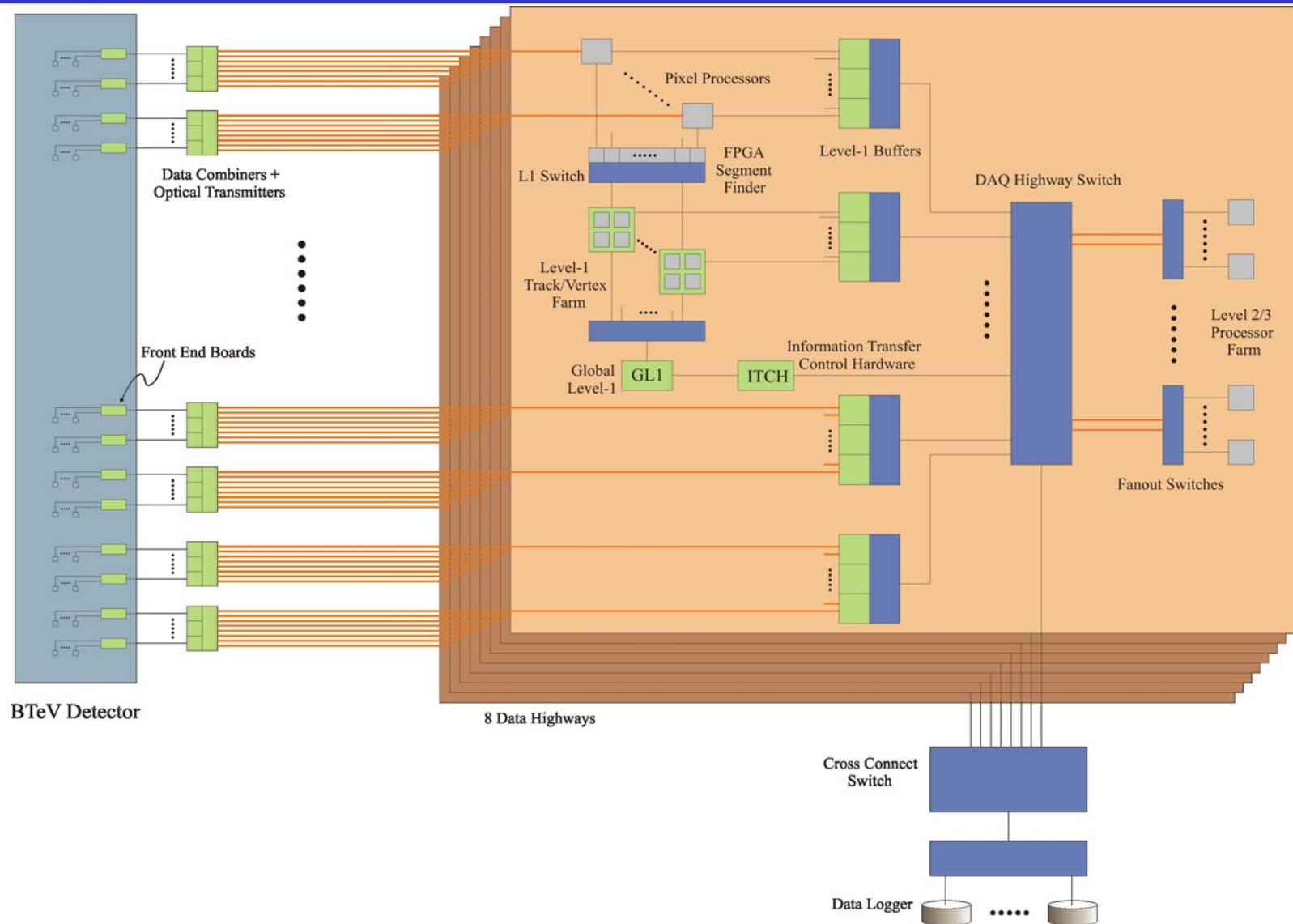
We have three phases of hardware development (pre-pilot, pilot, production), and two parallel packages of L2/3 software development beginning in FY05 and FY06, respectively.

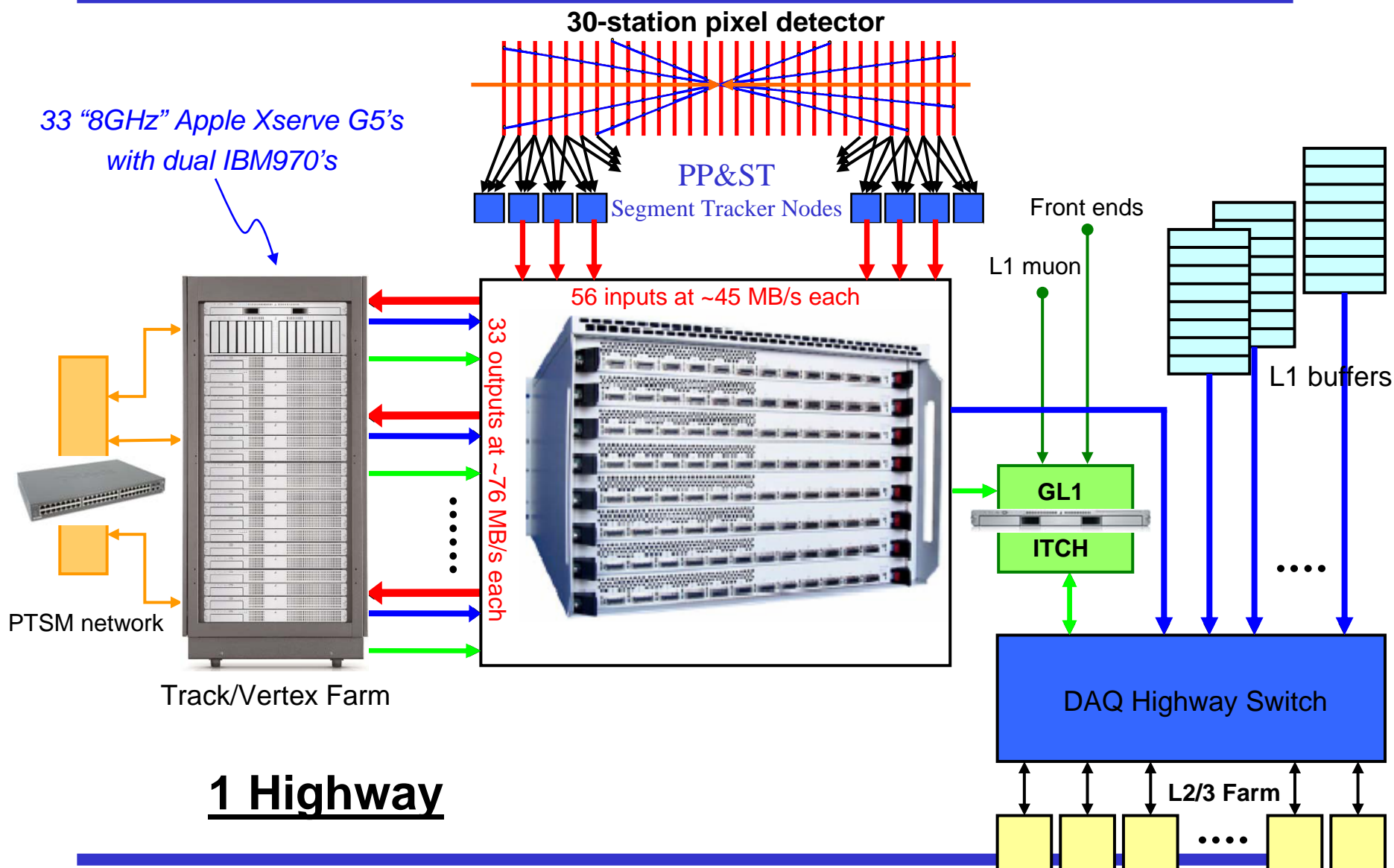
- L1 hardware and software (3-phase development)
 - Pre-pilot Switch & Farm (FY05) – hardware installation at FCC completed
 - Pilot (FY05 & FY06 with integration in FY07)
 - Production (begin 4-highway production in FY07)
- L2/3 hardware (3-phase development)
 - Pre-pilot (FY05 & FY06) – hardware installation at FCC completed
 - Pilot (5% in FY07)
 - Production (begin 4-highway production late in FY07)
- Software Package 1 – primarily L2 trigger code (development begins FY05)
 - L2 algorithm exists & satisfies efficiency, rejection, and timing requirements
 - Development effort is focused on detector alignment, framework, & utilities
- Software Package 2 – primarily L3 trigger code (development begins FY06)
 - L3 background rejection (factor of 2) is achievable with tracking detectors
 - Additional L3 algorithms are needed for online monitoring of data quality
 - L3 algorithms and online monitoring support BTeV physics analyses
 - L3 code development has scope contingency

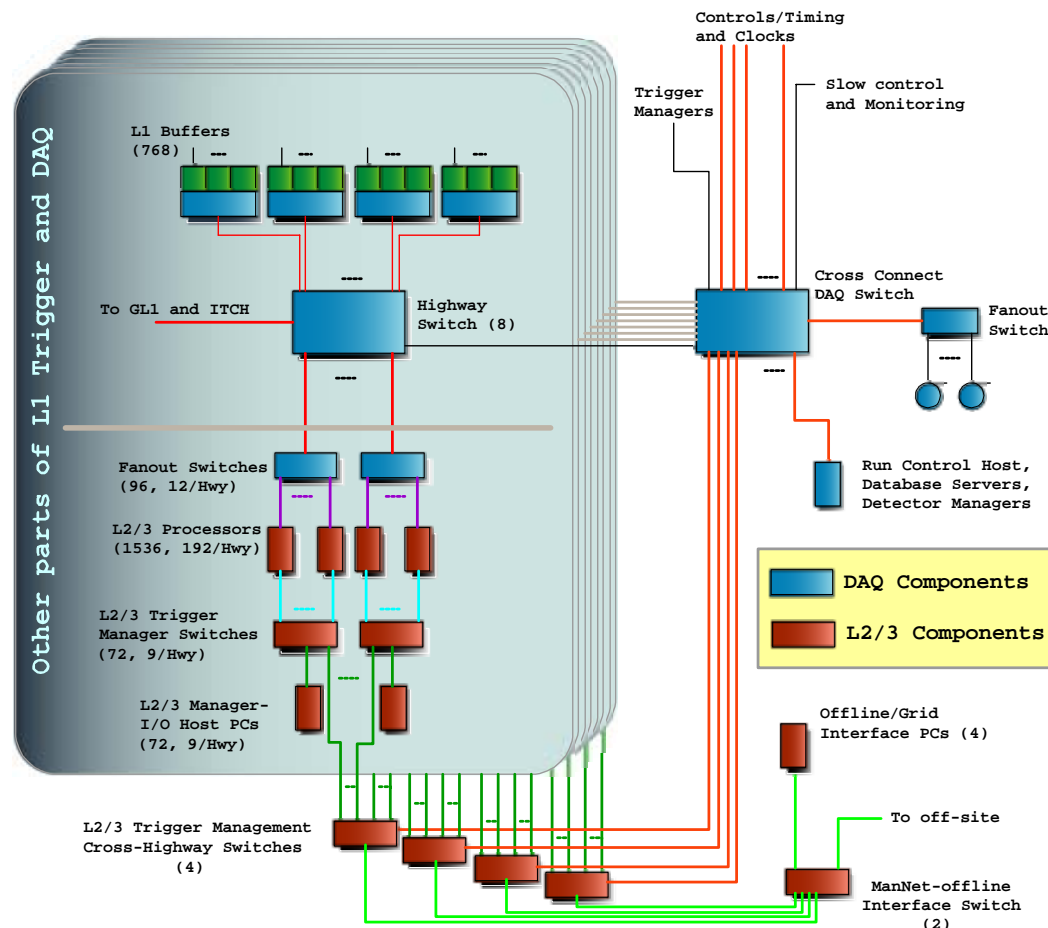
- Modified baseline architecture for L1, replacing two of three custom-designed trigger subsystems with commodity hardware. The revised WBS has “8 GHz” PowerPC processors (consistent with IBM roadmap) & Infiniband switches.
 - Performed L1 network simulations
 - Reviewed results in the trigger group
 - Presented results to BTeV Tech. Board
 - PCR approved: August 2004
- Purchased and installed 16 Apple G5 (dual 2 GHz) nodes and an Infiniband switch at Feynman Computing Center
- Started evaluation of real-time operating systems for the L1 trigger
- Acquired and installed a 100-node pre-pilot farm for the L2/3 trigger (located next to the L1 hardware).



Three-level, eight-highway data flow architecture







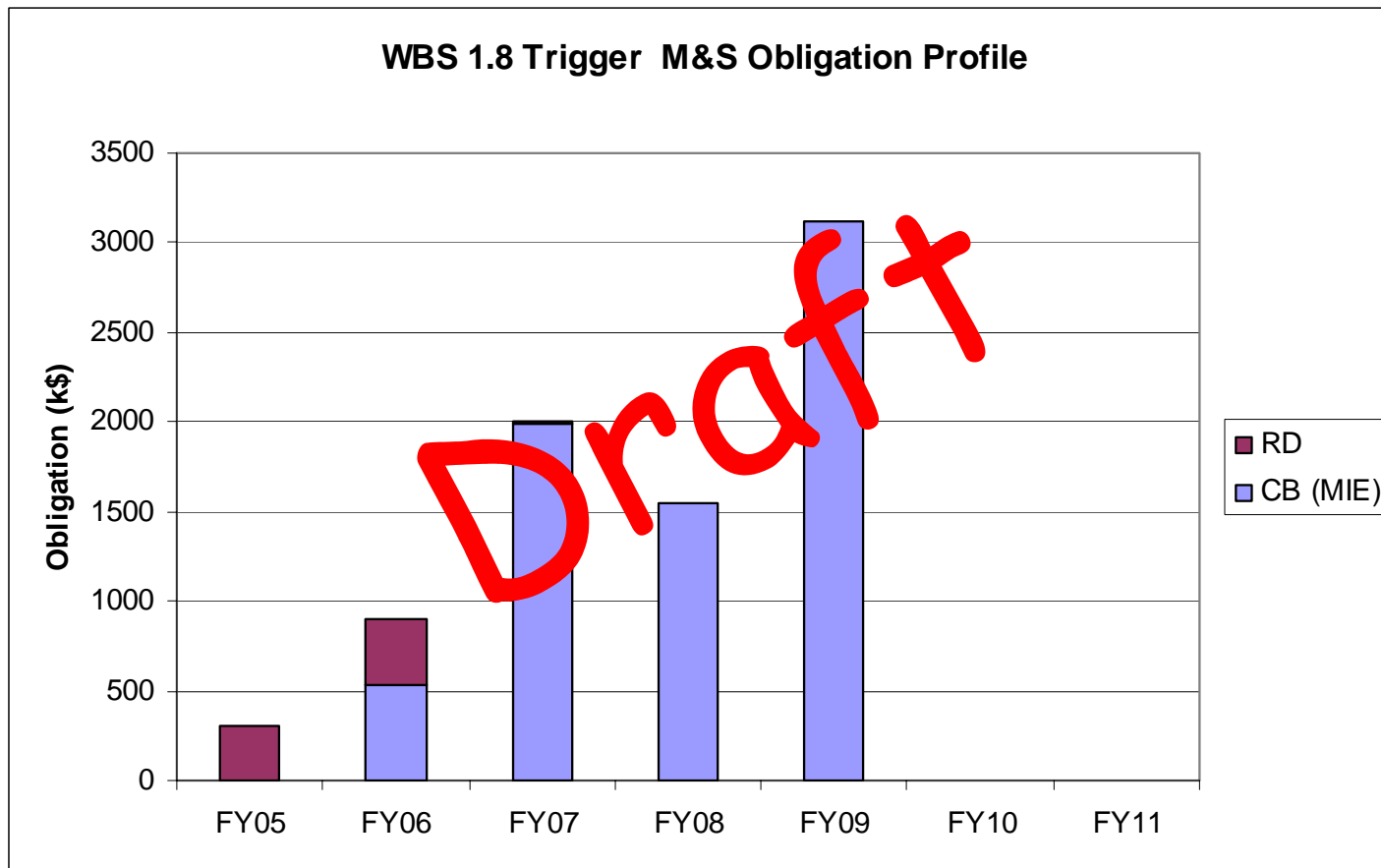
Baseline Design

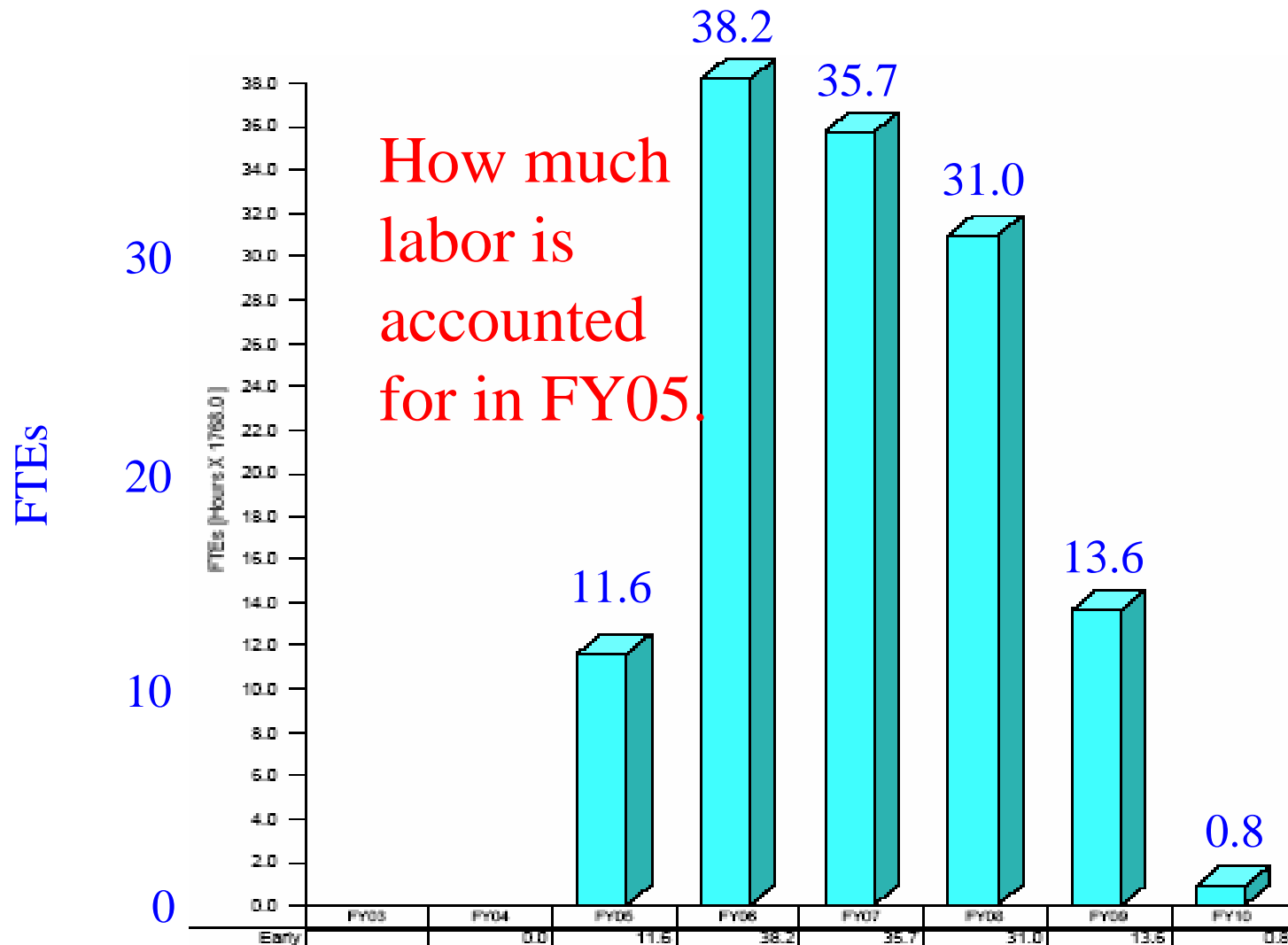
- L2/3 Processor farm consists of 1536 “12 GHz” CPUs (dual-CPU 1U rack-mount PCs)
- L2/3 trigger includes Manager-I/O Host PCs for database caches, worker management, monitoring, and event pool cache
- L2/3 Hardware in

- L2 and L3 reconstruction software (tracks, vertices, photons, π^0 's, hyperons, neutral kaons, particle identification)
- L2 and L3 trigger algorithms
- Global L2 and Global L3 software (trigger lists & selection criteria)
- Alignment and calibration software
- Monitoring, feedback and event display software
- Software framework, utilities, and interfaces to databases
- DAQ interface software
- Offline filter and fast charm/beauty monitoring software (high-level filtering and monitoring software)

Cost in FY05 dollars, fully burdened, includes both RD & MIE

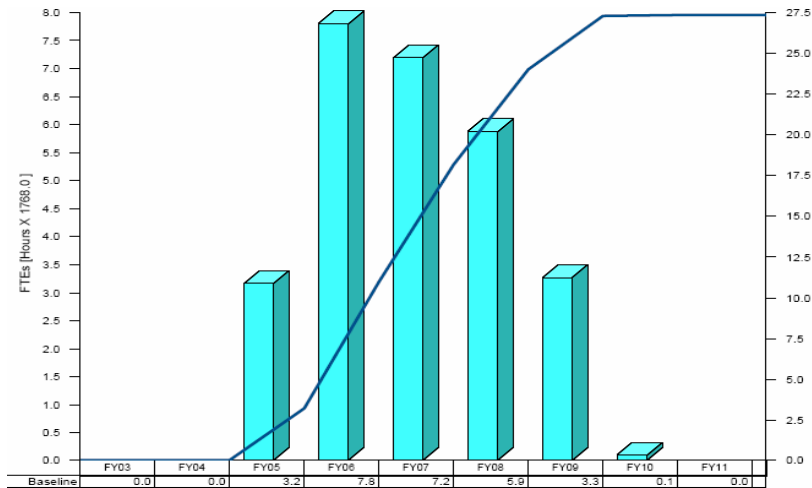
Activity ID	Activity Name	Base Cost (\$)	Material Contingency (%)	Labor Contingency (%)	Total FY05	Total FY06	Total FY07	Total FY08	Total FY09	Total FY10	Total FY05-10
1.8.1	L1 Hardware & Software	7,062,171	36	34	646,068	1,787,393	2,479,297	1,717,315	2,922,712	0	9,552,784
1.8.2	L2/L3 Hardware & Software	4,120,947	33	88	128,037	1,159,060	1,561,481	1,742,735	1,895,091	0	6,486,405
1.8.3	Trigger Electronics & SW Subproj Mgmt	230,199	3	24	46,879	48,439	52,287	53,737	53,570	19,399	274,311
1.8	file_18_07Dec04	11,413,318	35	61	820,983	2,994,892	4,093,066	3,513,787	4,871,373	19,399	16,313,500



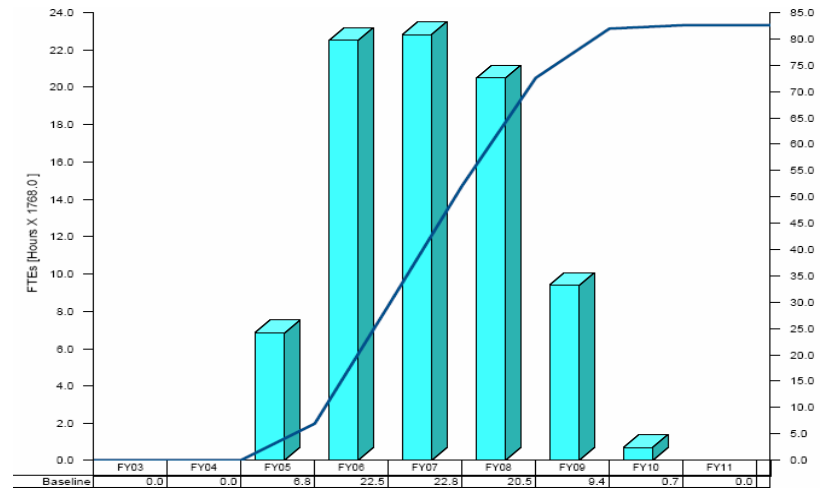


BTeV C₀ Labor Profiles by Fiscal Year (Base Plan) WBS 1.8

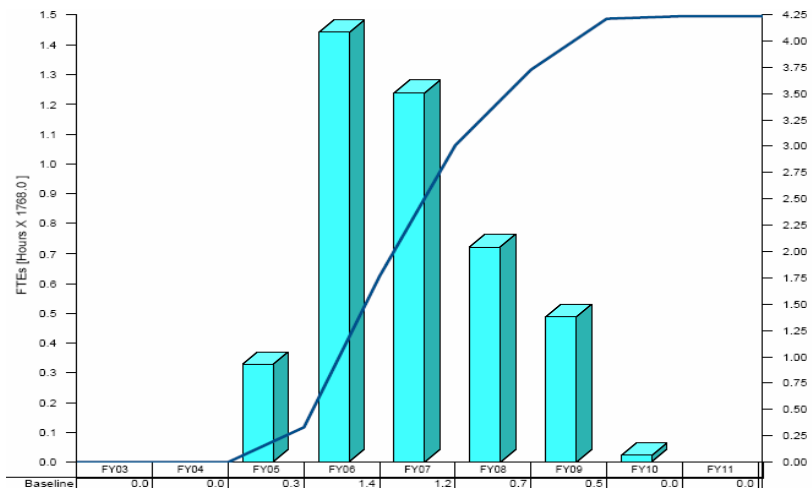
Technical Labor (Fermilab)



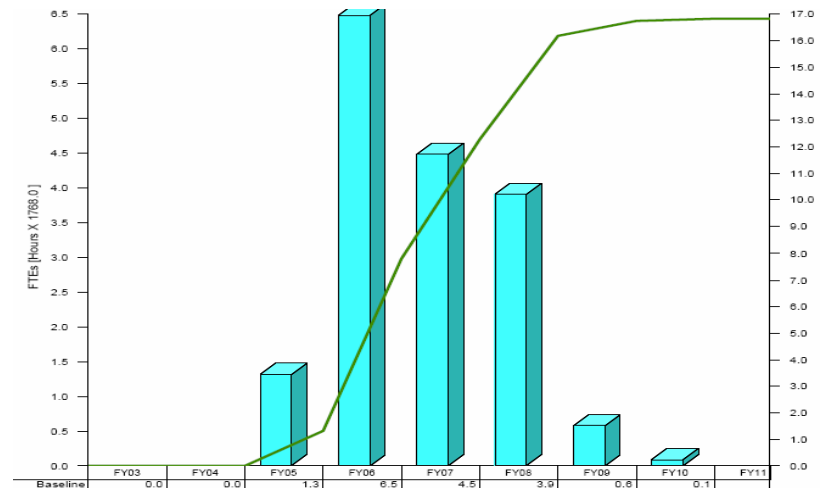
Physicist Labor (Fermilab)



Technical Labor (University)

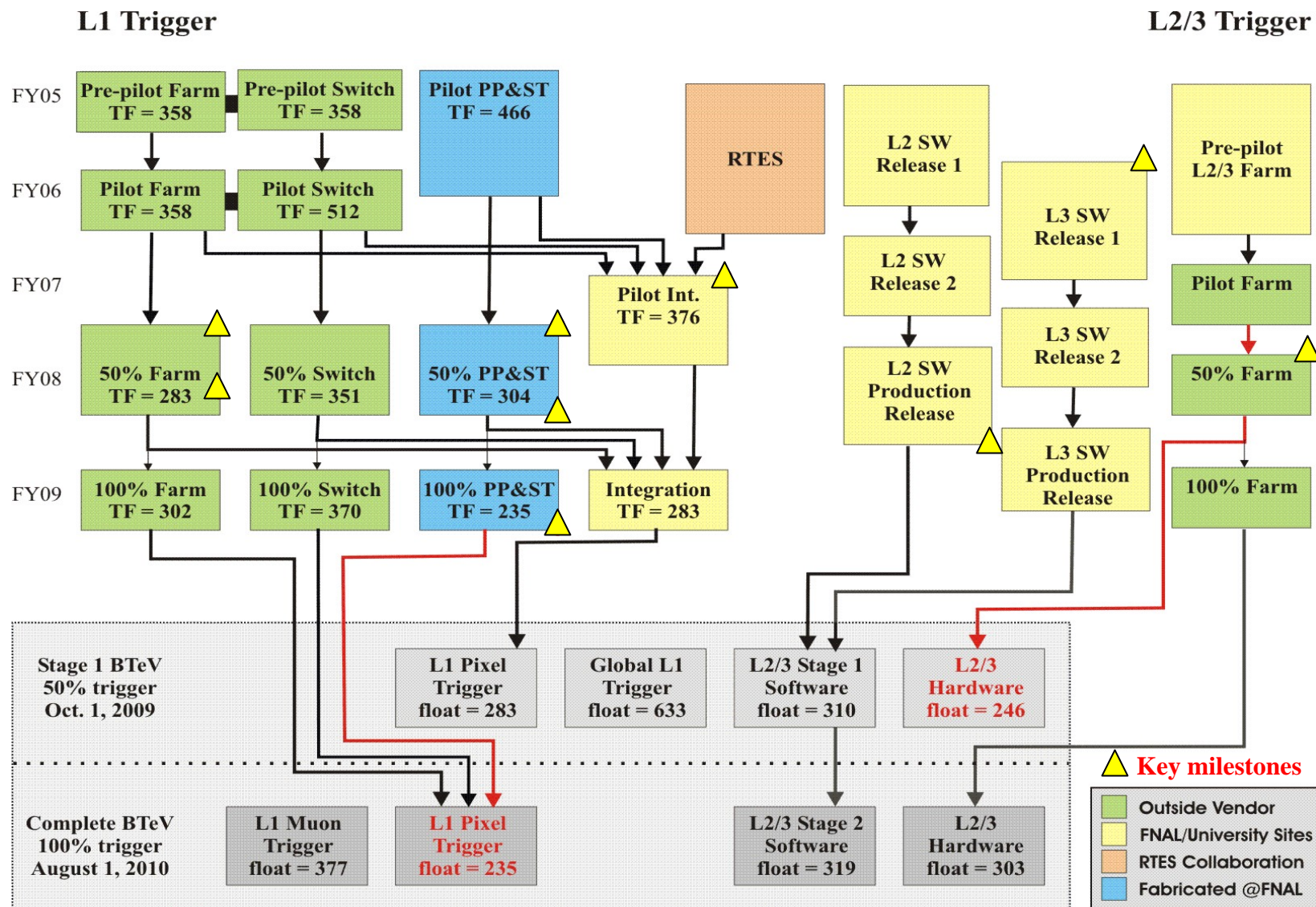


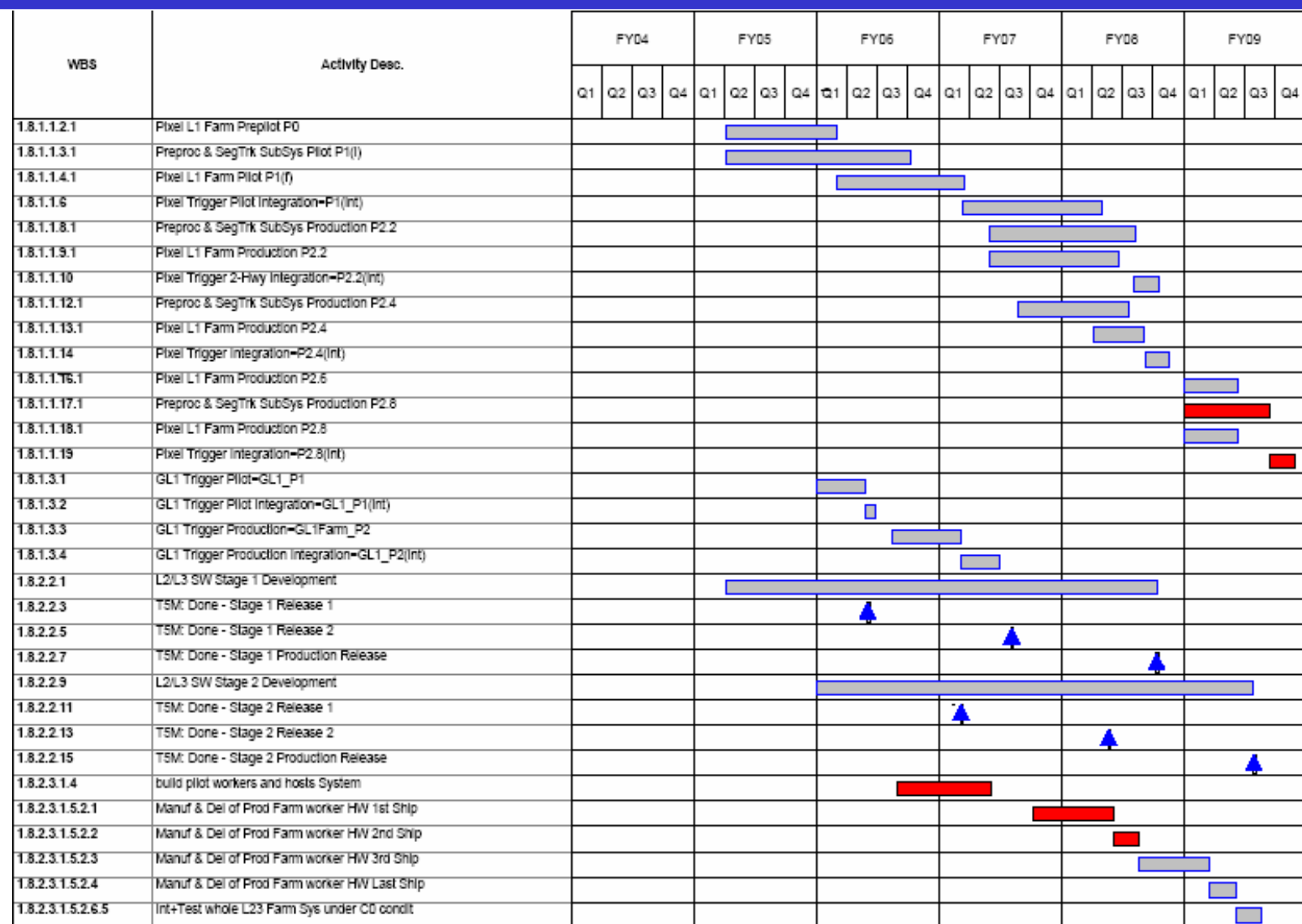
Physicist Labor (University)



- Multi-color labor plot (with table?)

- Labor ramp up for FY06 (moving from 2.5 to 15 FTE)
- Fractional effort in FY05 (6 people 50% or less), move to full time
- New institutions including DAQ in MOU (Houston, Iowa) in addition to OSU. Working on MOUs now. DOE approval should attract more or expand existing participation.
- New hire posting in FY05 to work off project, starting on BTeV in FY06
- Ongoing discussions with FNAL/CD management in identifying interest and expertise for FY06 effort, and project assignments are being made appropriately (eg, database and networking area).
- FNAL/CD technical staff has expressed interest and is keeping eyes on the project at a low level (more work would be happening in FY05 if funding resources were available).





- Stage 1 BTeV Trigger – 50% trigger system
 - Need-by date: October 1, 2009
 - Ready by October, 2008 (12 months of float)
 - 50% of L1 pixel trigger hardware (100% of L1 software)
 - 100% of Global Level 1 (GL1) hardware and software
 - 50% of L2/3 trigger hardware
 - Final production release of Package 1 software (L2 code complete)
 - Second release of Package 2 software
- Stage 2 BTeV Trigger – 100% trigger system
 - Need-by date: August 1, 2010
 - Ready by September, 2009 (11 months of float)
 - Remaining 50% of L1 and L2/3 trigger hardware
 - 100% of L1 muon trigger
 - Final production release of Package 2 software (L3 code complete)

- Stage 1 BTeV trigger (246 workdays of float)
 - Completing the first four highways for the L2/3 trigger has the lowest total float for the **Stage 1 BTeV detector**, with 246 days of float. The activities involve the procurement of computer farms. Procurement is delayed to obtain more processing capabilities for lower cost. The procurement of processors for the L2/3 trigger has minimal schedule risk, and there is considerable expertise for this work at Fermilab.
- Stage 2 BTeV trigger (235 workdays of float)
 - The completion of the remaining four highways of the L1 pixel preprocessor and segment tracker (PP&ST) hardware has the lowest total float for the **Stage 2 BTeV detector**, with 235 days of float. By the time this work is started we will have considerable expertise building, testing, and commissioning PP&ST hardware. Therefore, we expect minimal schedule risk, since four trigger highways will be fully operational by the time this work begins.

Activity Desc.	Early Finish	Baseline - PMB	FY05				FY06				FY07				FY08				FY09				FY10				FY11			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
T0M: CD-1 Approve Preliminary Baseline Range	30Dec04	30Dec04	▲																											
T0M: CD-2 Approve Performance Baseline	31Mar05	31Mar05		▲																										
T0M: CD-3a Approve Limited Construction	31Mar05	31Mar05		▲																										
T0M: CD-3b Approve Start of Construction	30Sep05	30Sep05				▲																								
T3M-60: Start L3 software development	03Oct05	03Oct05				▲																								
T2M-17: Trigger pilot system ready for testing	11Dec06	31Aug07									▲		▲																	
T3M-55: Start L1 2-hgwy pixel proc/seg trkr prod	01Mar07	04Sep07										▲		▲																
T3M-57: Start L1 2-highway farm production	01Mar07	04Sep07										▲		▲																
T3M-59: Start L2/L3 farm worker node procurement	09Jul07	02Jan08											▲		▲															
T3M-58: End L1 2-highway farm production	18Mar08	16Dec08													▲		▲													
T3M-56: End L1 2-hgwy pixel proc/seg trkr prod	06May08	10Feb09													▲		▲													
T2M-18: 1st prod release: Lvl 2/3 Trig software	10Jul08	02Mar09														▲		▲												
T3M-61: 1st prod release: Lvl 2/3 Trig software	10Jul08	02Mar09														▲		▲												
T3M-62: Trig sys & integration with DAQ complete	24Aug09	18Feb10																	▲		▲									
T0M: CD-4 Approve Start of Ops - Project Closeout	30Jun11	30Jun11																											▲	

WBS Item	Risk Event	Response/Mitigation Strategy
For example: 1.8.1.1.2.1, 1.8.1.1.4.1	Baseline processor fails to meet requirements	Benchmark and qualify more than one processor during R&D or early construction phase. Have a 2 nd option ready if the 1 st option is unsatisfactory.
For example: 1.8.1.1.8.1.1.1, 1.8.1.2.1.2	Pixel segment tracker or muon preprocessor algorithm exceeds the size of the selected FPGA. Larger FPGA increases the cost	Use contingency funds to upgrade to a bigger and more expensive FPGA. Consider other implementation alternatives early in the design stage. Consider simplifying the algorithms.
For example: 1.8.1.1.3.1.1.1, 1.8.1.1.8.1.1.1	Communication links do not satisfy error rate specifications	Use contingency to modify PC boards, buy new parts, connectors, or cables.
For example: 1.8.1.1.4.1.1.5, 1.8.2.2	Shortage of software developers	Prioritize critical tasks. Use contingency to hire software developers.
Numerous WBS items	Experienced people leave the trigger project.	Be sure that more than one person is working on critical tasks. Use contingency funds to hire the person who leaves as a temporary consultant, and transfer their expertise to existing or new personnel.

- Develop a schedule which (a) completes critical design and validation activities as soon as possible and is ready for production six to nine months in advance of the production start date, and (b) completes production of the trigger and data acquisition systems six to nine months in advance of first collisions.
 - (a) Critical design and validation activities have been an ongoing effort. We will complete the L1 PP&ST system 8 months before the start of production.
 - (b) We have developed a schedule that completes 50% of the L1 trigger more than 13 months before the need-by date for the Stage 1 detector, and completes 50% of the L2/3 trigger almost one year before the need-by date.
- Re-evaluate the basis of estimate of the FPGA costs to allow for uncertainty in the de-escalation profile.
 - We no longer de-escalate FPGA costs.
- Quickly identify and apply new individuals and groups to provide the physicist effort for by the WBS.
 - We have identified new individuals and groups (Univ. of Houston, Southern Methodist University, Univ. of Virginia), and are continuing to do so.

- L1 Pixel Preprocessor & Segment Tracker (PP&ST) Pilot – (RD)
 - Develop specifications for the PP&ST subsystem
 - Design, simulate, and develop firmware for Pilot PP&ST trigger highway
- L1 Trigger Pre-pilot Switch and Farm – (RD & PED)
 - Purchase & install 16-node Apple G5 Pre-pilot Farm
 - Evaluate real-time operating system software for L1 Farm
 - Continue development of L1 trigger algorithm & L1 software framework
 - Purchase additional hardware for Pre-pilot engineering design effort
- L2/3 Trigger Software – (RD & PED)
 - Develop L2 trigger methods and evaluate L2 trigger algorithms
 - Develop L2 trigger pre-production software
 - Develop Global L2 pre-production software
 - Develop L2 specifications (framework, alignment, calibration, utilities)

- Our team has a history of taking on difficult problems and solving them. Over time this has helped us develop the technical expertise that is needed to build the BTeV trigger.
- Examples of some of our achievements:
 - Developed a detached L1 vertex trigger for B physics in a hadron collider
 - Influenced pixel detector design by developing new L1 trigger algorithms (2-plane algorithm, “inner” & “outer” tracking, “exterior” hit elimination)
 - Implemented the L1 pattern recognition algorithm in FPGA hardware
 - Designed and built a multi-processor DSP prototype system
 - Developed expertise in low-level assembly language programming (DSPs)
 - Introduced concept of “highways” to simplify the trigger/DAQ architecture
 - Developed L2 algorithm that meets efficiency, rejection, timing requirements
 - Introduced commodity hardware as a replacement for DSP processing farm
- We are ready to move from prototype to system development, and have started to assemble a pre-pilot trigger highway for L1 and L2/3.
- Our cost and schedule for the development and construction of the BTeV trigger is robust and achievable, and has benefited from the feedback that we have received from past reviews.

More information on the BTeV trigger is available in these presentations:

WBS 1.8

- L1 pixel trigger – Vince Pavlicek
- L1 muon trigger – Mike Haney
- Global Level 1 – Vince Pavlicek
- L2/3 software – Paul Lebrun
- L2/3 hardware – Harry Cheung

Additional Slides

DCB	Data Combiner Board
DDR	Double Data Rate
FCC	Feynman Computing Center
FPGA	Field Programmable Gate Array
GBE	Gigabit Ethernet
GL1	Global Level 1
Infiniband	Third generation high-speed networking standard
ITCH	Information Transfer Control Hardware
L1B	Level 1 Buffer
L2/3 Package 1	Components needed to complete software for L2 trigger
L2/3 Package 2	Components needed to complete software for L3 trigger
PCI	Peripheral Component Interface
PCI-Express	High-speed serial version of PCI
PCR	Project Change Request
PP&ST	Pixel Preprocessor and Segment Tracker
PTSM	Pixel Trigger Supervisor and Monitor
RCS	Run Control System
RTES	Real-Time Embedded Systems
Xserve G5	Apple's PowerPC based 1U server with dual 64-bit processors

T2	Trigger pilot system tested	Jan-07
T2,T3	Stage 1 production release of L2/3 software	Jul-08
T3	Begin L1 2-highway pixel processor & segment tracker production	Mar-07
T3	End L1 2-highway pixel processor & segment tracker production	May-08
T3	Begin L1 2-highway farm production	Mar-07
T3	End L1 2-highway farm production	Mar-08
T3	Begin L2/3 farm worker node procurement	Jul-07
T3	Begin L3 software development	Oct-05
T3	Complete trigger system and integration with DAQ	Aug-09

T2	Trigger pilot system tested	Jul-07
T2,T3	Stage 1 production release of L2/3 software	Mar-09
T3	Begin L1 2-highway pixel processor & segment tracker production	Jul-07
T3	End L1 2-highway pixel processor & segment tracker production	Dec-08
T3	Begin L1 2-highway farm production	Jul-07
T3	End L1 2-highway farm production	Oct-08
T3	Begin L2/3 farm worker node procurement	Jan-08
T3	Begin L3 software development	Oct-05
T3	Complete trigger system and integration with DAQ	Feb-10

